NEW HIGH-END ARCHITECTURE

Originally published in the article "Multimedia ICs advanace in both high and consumer ends" by Rodney Myrvaagnes. Source: http://www.electronicproducts.com/Digital_ICs/Multimedia_ICs_advance_in_both_high_and_consumer_ends.aspx

A new architecture has appeared to compete for the high-end media-processor market. Bops (Palo Alto, CA) — a licensing firm formed to continue the M-fast project discontinued by IBM — has launched the Manifold Array (ManArray), an array-processor architecture that is extensible in both torus and hypercube topologies.

By licensing its design to semiconductor makers in the same way that Advanced RISC Machines (Los Gatos, CA) does, for example, the company hopes to enter the same market as the Chromatic Research (Sunnyvale, CA) Mpact and the Philips Semiconductors (Sunnyvale, CA) Trimedia programmable media processors. Bops will retain control of the instruction set, which all licensees will be contracted to follow. Unlike Chromatic, Bops will publish the instruction set so that anyone can write applications or develop tools.

The ManArray structure is derived from a fully connected 4 x 4 torus of processing elements (PEs). A series of row and column transpositions ends with each row of four cells containing two cells with their respective transposes. For example, cells (2,0) (1,1) (0,2), and (3,3) come together.

Furthermore, all communications between rows are now either north and west or south and east. The row of four is physically put into a 2 x 2 block to make the basic die design, with the external connections combined in a single bus from both the north-and-west and the south-and-east wires.

Bringing all cells adjacent to their transposes reduces the data delay between them to one cycle. Many common DSP processes — such as FFTs, matrix transpositions and multiplications, and discrete cosine transforms (DCTs) — transpose data elements and thus benefit from the ManArray topology. When 2 x 2 clusters are joined to make larger clusters, PE-to-PE communication between adjacent clusters remains one cycle.

The PEs are joined and controlled by a sequence processor (SP). The SP, a superset of the PE, includes a fully connected crossbar (cluster switch) joining the four PEs on the chip (see figure 1). When multiple chips are used in SIMD mode, the SP on one of the chips can control PEs on other chips that are executing the same instruction stream.

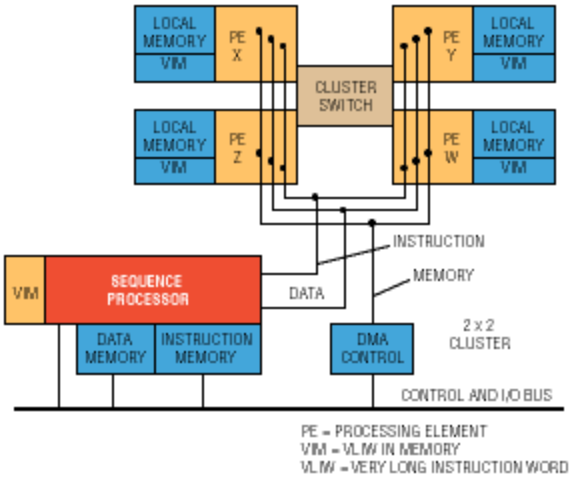

Fig. 1. The basic ManArray building block is a 2 x 2 cluster of processing elements, controlled by a sequence processor and a cluster switch.

Alternatively, when a series of operations must be done on each member of a large data array, PEs or groups of PEs can be connected sequentially as an ad-hoc pipeline. This reconnection is entirely software controlled, using the SPs, and can be done in the same physical machine as the torus or hypercube SIMD.

The internal logic of the PE has load-store capability like a normal microprocessor, but it also has the capability of storing reusable lines of instructions, grouped into encapsulated very-long-instruction words (eVLIW) (see figure 2). When an algorithm has been debugged and its operation is well understood, up to five instructions that can execute simultaneously may be usefully grouped into each VLIW and stored in the VLIW instruction memory (VIM). Then, each time the VLIW is needed, it is invoked by a single 32-bit instruction in the input stream.

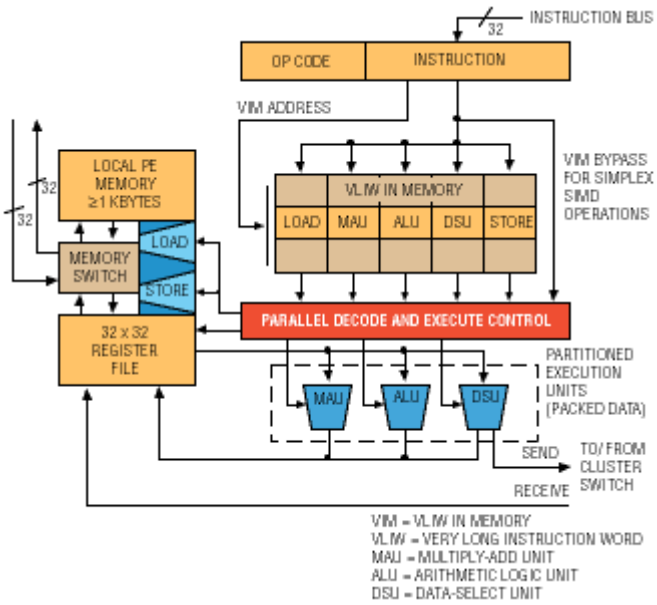

Fig. 2. Instructions for the ManArray's processing elements come in 32-bit words, but groups of operations that can execute simultaneously may be stored in the VLIW memory and rerun by a single instruction.

Programming the ManArray can start with sequential code like any DSP or microprocessor. When that is debugged, packed data types may be introduced where appropriate.

Examination of the code will identify combinations of execution units used inside loops. These can then be grouped into eVLIWs that initialize, run, and empty a pipeline.

The initial ManArray chip, called Kitty Hawk, will be a 2 x 2 cluster. It is expected to be introduced in the first half of 1998.

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